KYOCERA

LV-PECL or LVDS/ 3.3V or 2.5V/ 5.0×3.2mm

RoHS Compliant

Features

- High frequency to 800MHz
- LV-PECL output or LVDS output
- Miniature ceramic package
- Compact and low profile (5.0×3.2×1.2mm max.)
- Low current consumption

Applications

- WDM/ Networking

Table 1

Freq. Tol. Code	Freq. Tol. × 10^{-6}	Operating Temperature Range (°C)	Note
G	±50	−40 to +85	Please contact us for available frequencies.

How to Order

KV5032R 622.080 □ □ G D 00
① ② ③ ④ ⑤ ⑥ ⑦

①Series
②Output Frequency
③Output Type (P : LV-PECL or L : LVDS)
④Supply Voltage (3 : 3.3V or 2 : 2.5V)
⑤Frequency Tolerance (See Table 1)
⑥Symmetry/ INH Function
(45/ 55%, Disable)
⑦Individual Specification
(STD Specification is "00".)

Packaging (Tape & Reel 1000 pcs./ reel)

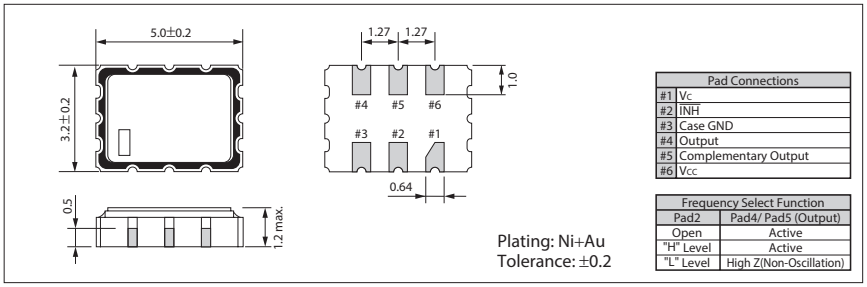
Specifications

Item	Symbol	Conditions		Min.	Max.	Unit
Output Frequency Range[Note1]	fo			10	800	MHz
Frequency Tolerance	f_tol	Initial tolerance, Operating temperature range, Rated power supply voltage change, Load change, Aging (1 year @25°C), Shock and vibration	Temp.: −40 to +85°C	−50	+50	×10^{-6}
Absolute Pull Range	APR			±100	—	×10^{-6}
Control Voltage	Vc			0	+3.3	V
Storage Temperature Range	T_stg			−55	+125	°C
Operating Temperature Range	T_use			−40	+85	°C
Max. Supply Voltage	—			−0.5	+4.2	V
Supply Voltage	Vcc			+2.25	+2.75	V
				+2.97	+3.63	
Linearity	—	Vc=0V to +3.3V		−10	10	%
Current Consumption	Icc	LV-PECL Output (2.25≤Vcc≤2.75V)		—	80	mA
		LV-PECL Output (2.97≤Vcc≤3.63V)		—	100	
		LVDS Output (2.25≤Vcc≤2.75V, 2.77≤Vcc≤3.63V)		—	40	
Symmetry	SYM	LV-PECL Output 50ohm @crossing point		45	55	%
		LVDS Output 100ohm @crossing point		45	55	
Rise/ Fall Time (20% to 80% Output Level)	Tr/ Tf	LV-PECL Output 50ohm		—	0.4	ns
		LVDS Output 100ohm		—	0.6	
Low Level Output Voltage[Note2]	VOL	LV-PECL Output		—	Vcc −1.620	V
High Level Output Voltage[Note2]	VOH			Vcc −1.025	—	V
Output Load	—			50		ohm
Low Level Output Voltage[Note2]	VOL	LVDS Output	Typ. 1.1V	0.9	—	V
High Level Output Voltage[Note2]	VOH		Typ. 1.43V	—	1.6	V
Diffrentical Output Voltage[Note2]	VOD		Typ. 330mV	175	454	mV
Diffrentical Output Voltage Error[Note2]	dVOD		dVOD= |VOD1−VOD2|	—	50	mV
Offset Voltage	VOS		Typ. 1.25V	1.125	1.375	V
Offset Voltage Error	dVOS		dVOS= |VOS1−VOS2|	—	50	mV
Output Load	—			100		ohm
Low Level Input Voltage[Note2]	VIL			—	30% Vcc	V
High Level Input Voltage[Note2]	VIH			70% Vcc	—	V
Input Resistance	—			150	—	k ohm
Disable Time	t_dis			—	200	ns
Enable Time	t_ena			—	2	ms
Start-up Time	t_str	@Minimum operating voltage to be 0 sec.		—	10	ms
Phase Jitter	Jphase	@622.08MHz	BW : 12kHz to 20MHz	Typ. 3.0		ps
Phase Noise	—	@622.08MHz	@10Hz offset	Typ. −40		dBc/ Hz
			@100Hz offset	Typ. −70		
			@1kHz offset	Typ. −95		
			@10kHz offset	Typ. −105		
			@100kHz offset	Typ. −105		
			@1MHz offset	Typ. −125		
			@10MHz offset	Typ. −135		

Note : All electrical characteristics are defined at the maximum load and operating temperature range.
Note1: Please contact us for inquiry about operating temperature range, available frequencies and other conditions. Note2: DC characteristic

Dimensions

(Unit: mm)



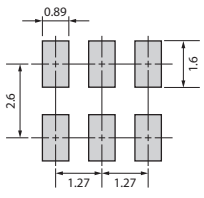
Plating: Ni+Au
Tolerance: ±0.2

Pad Connections	
#1	Vc
#2	INH
#3	Case GND
#4	Output
#5	Complementary Output
#6	Vcc

Frequency Select Function	
Pad2	Pad4/ Pad5 (Output)
Open	Active
"H" Level	Active
"L" Level	High Z(Non-Oscillation)

Recommended Land Pattern

(Unit: mm)



Note: 0.01μF capacitor between Vcc and GND is recommended for bypass purpose.