



LV-PECL or LVDS/ 3.3V or 2.5V/ 5.0x3.2mm



RoHS Compliant

Features

- High frequency to 900MHz
- LV-PECL output or LVDS output
- Miniature ceramic package
- Compact and low profile (5.0x3.2x1.2mm max.)
- Low current consumption

Applications

- WDM/ Networking

Table 1

Freq. Code	Tol. $\times 10^{-6}$	Operating Temperature Range (°C)	Note
G	± 50	-40 to +85	Please contact us for available frequencies.

How to Order

KC5032R 622.080 G D 00
 ① ② ③ ④ ⑤ ⑥ ⑦

- ① Series
- ② Output Frequency
- ③ Output Type (P : LV-PECL or L : LVDS)
- ④ Supply Voltage (3 : 3.3V or 2 : 2.5V)
- ⑤ Frequency Tolerance (See Table 1)
- ⑥ Symmetry/ INH Function (45/ 55%, Disable)
- ⑦ Individual Specification (STD Specification is "00")

Packaging (Tape & Reel 1000 pcs./ reel)

Specifications

Item	Symbol	Conditions	Min.	Max.	Units
Output Frequency Range ^{Note1}	f _o		10	900	MHz
Frequency Tolerance	f _{tol}	Initial tolerance, Operating temperature range, Rated power supply voltage change, Load change, Aging (1 year @25°C), Shock and vibration Op. Temp.: -40 to +85°C	-50	+50	$\times 10^{-6}$
Storage Temperature Range	T _{stg}		-55	+125	°C
Operating Temperature Range	T _{use}		-40	+85	°C
Max. Supply Voltage	—		-0.5	+4.2	V
Supply Voltage	V _{cc}		+2.25 +2.97	+2.75 +3.63	V
Current Consumption	I _{cc}	LV-PECL Output (2.25 ≤ V _{cc} ≤ 2.75V) LV-PECL Output (2.97 < V _{cc} < 3.63V) LVDS Output (2.25 ≤ V _{cc} ≤ 2.75V, 2.97 ≤ V _{cc} ≤ 3.63V)	— — —	80 100 40	mA
Symmetry	SYM	LV-PECL Output 50ohm @crossing point LVDS Output 100ohm @crossing point	45 45	55 55	%
Rise/ Fall Time (20% to 80% Output Level)	t _r / t _f	LV-PECL Output 50ohm LVDS Output 100ohm	— —	0.4 0.6	ns
Low Level Output Voltage ^{Note2}	V _{OL}		—	V _{cc} - 1.620	V
High Level Output Voltage ^{Note2}	V _{OH}	LV-PECL Output	V _{cc} - 1.025	—	V
Output Load	—		—	50	ohm
Low Level Output Voltage ^{Note2}	V _{OL}		Typ. 1.1V	0.9	V
High Level Output Voltage ^{Note2}	V _{OH}		Typ. 1.43V	—	V
Differential Output Voltage ^{Note2}	V _{OD}		Typ. 330mV	175	mV
Differential Output Voltage Error ^{Note2}	dV _{OD}	LVDS Output dV _{OD} = V _{OD1} - V _{OD2}	—	50	mV
Offset Voltage	V _{OS}		Typ. 1.25V	1.125	V
Offset Voltage Error	dV _{OS}	dV _{OS} = V _{OS1} - V _{OS2}	—	50	mV
Output Load	—		—	100	ohm
Low Level Input Voltage ^{Note2}	V _{IL}		—	30% V _{cc}	V
High Level Input Voltage ^{Note2}	V _{IH}		70% V _{cc}	—	V
Disable Time	t _{dis}		—	200	ns
Enable Time	t _{ena}		—	2	ms
Start-up Time	t _{str}	@Minimum operating voltage to be 0 sec.	—	10	ms
Phase Jitter	J _{Phase}	@622.08MHz BW : 12kHz to 20MHz @10Hz offset @100Hz offset @1kHz offset @10kHz offset @100kHz offset @1MHz offset @10MHz offset	—	Typ. 3.0 Typ. -40 Typ. -70 Typ. -95 Typ. -105 Typ. -105 Typ. -125 Typ. -135	ps
Phase Noise	—	@622.08MHz	—	—	dBc/ Hz

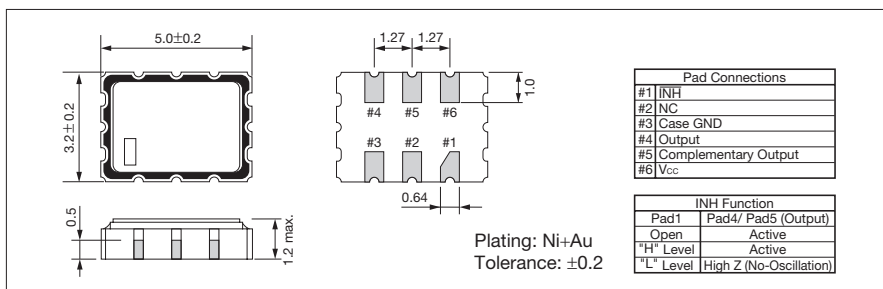
Note : All electrical characteristics are defined at the maximum load and operating temperature range.

Note1: Please contact us for inquiry about operating temperature range, available frequencies and other conditions.

Note2: DC characteristic

Dimensions

(Unit: mm)



Recommended Land Pattern

(Unit: mm)

