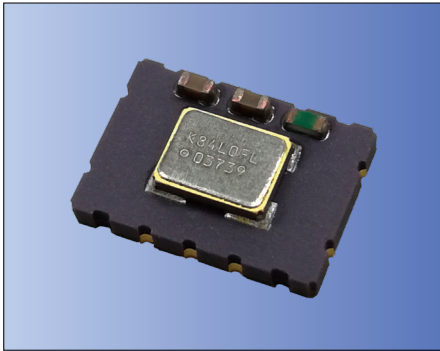




7.0×5.0mm



RoHS Compliant

**Features**

- High stability and high reliability
- 2.3 to 3.63V drive available
- Clipped sine wave or CMOS level output
- Low phase noise
- Disable Function (KT7050A)
- Operating Temp. -40 to +105°C (Option)

**Applications**

- 5G, Smallcell, Stratum3
- SONET/ SDH/ Ethernet
- SyncE/ IEEE 1588

**How to Order**

KT7050 □ 20000 □ □ □ 33 T xx  
① ② ③ ④ ⑤ ⑥ ⑦ ⑧

①Series

③Output Frequency

④Freq. Temp. Chrst.

U	±0.5×10 <sup>-6</sup>
K	±0.28×10 <sup>-6</sup>
A	±0.1×10 <sup>-6</sup>

⑥Supply Voltage

33	3.3V
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②Land Type

A	10Pads
B	4Pads

⑤Operating Temperature Range

GT	-10°C to 70°C
AW	-40°C to 85°C
AY	-40°C to 105°C

⑦Voltage Control Function

T	TCXO
Spec. Code*	VCTCXO

\*Please contact us for Spec. Code.

⑧Individual Specification

Packaging (Tape & Reel 1000 pcs./ reel)

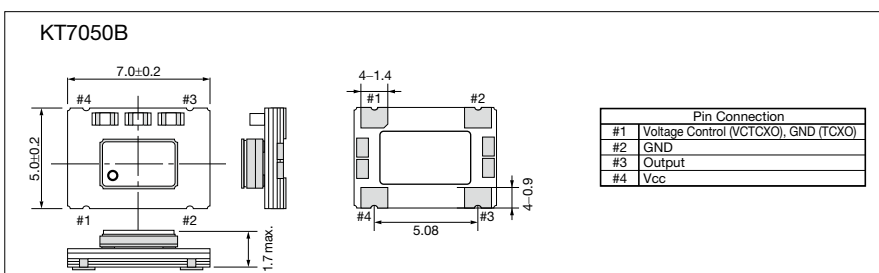
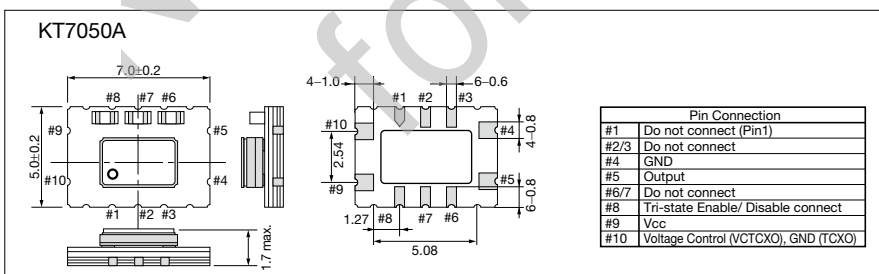
- Compliant to the GR1244-Core & GR253-Core
- Recommended in Microsemi's ZLAN-68 app. note for Stratum3 applications based on tests performed by Kyocera.

**Specifications**

Item	Symbol	Conditions	Min.	Max.	Unit	
Output Frequency Range	f <sub>o</sub>	Standard Frequency: 10 / 12.8 / 20 / 25.6 / 44.8	10	44.8	MHz	
Frequency Tolerance	f <sub>tol</sub>	vs Temperature [±(f <sub>max</sub> -f <sub>min</sub> )/ 2f <sub>o</sub> ]	-0.5	+0.5	×10 <sup>-6</sup>	
		vs Voltage	-0.28	+0.28		
Supply Voltage	V <sub>CC</sub>		+2.3	+3.63	V	
Current Consumption	I <sub>CC</sub>	CMOS Output	—	6	mA	
Frequency Aging	f <sub>age</sub>	20years aging @40°C Including temp characteristics, initial tolerance, rated power supply voltage change and load change.	-4.6	+4.6	×10 <sup>-6</sup>	
Voltage Control Range	f <sub>cont</sub>	Positive *100k ohm min	±5	±20	×10 <sup>-6</sup>	
Output Level	V <sub>pp</sub>	Clipped Sine, Load: 10k ohm // 10pF	0.8	—	Vp-p	
Low Level Output Voltage	V <sub>OL</sub>	CMOS, Load: 15pF I <sub>OL</sub> =4mA	—	10% V <sub>CC</sub>	V	
High Level Output Voltage	V <sub>OH</sub>	CMOS, Load: 15pF I <sub>OH</sub> =-4mA	90% V <sub>CC</sub>	—	V	
Rise / Fall Time (10%V <sub>CC</sub> to 90%V <sub>CC</sub> )	Tr/ Tf	CMOS, Load: 15pF	—	8	ns	
Symmetry	SYM	50% V <sub>CC</sub>	45	55	%	
Phase Noise	—	@20MHz	@10Hz offset	—	-90	dBc/ Hz
			@100Hz offset	—	-120	
			@1kHz offset	—	-140	
			@10kHz offset	—	-150	
			@100kHz offset	—	-150	

\* Please contact us for other specifications.

**Dimensions**



**Recommended Land Pattern**

(Unit: mm)

